The following listing of claims will replace all prior versions, and listings, of claims in the present application:

LISTING OF CLAIMS:

Claim 1 (Currently Amended) A method of forming a double-gate transistor comprising the steps of:

providing a semiconductor wafer having a substrate and a device layer, a back gate dielectric layer adjacent to and below said ~~Device~~ device layer, a back gate electrode between said back gate dielectric layer and said substrate, a front gate dielectric on said ~~Device~~ device layer and a front gate electrode layer on said front gate dielectric layer;

depositing at least one transfer layer on said front gate electrode layer;

patterning said at least one transfer layer with a gate pattern and forming a first gate in said front gate electrode layer using said transfer layer as a mask;

forming at least one vertical spacer layer adjacent to opposite sides of said front gate;

etching said ~~Device~~ device layer using said at least one spacer layer as a mask to form a transistor body disposed on said back gate dielectric layer;

oxidizing said back gate electrode such that oxide is formed below said transistor body and on either side of a central portion of said back gate electrode, thereby forming said back gate self-aligned with said front gate; and

forming source and drain electrodes on opposite sides of said transistor body.

Claim 2 (Currently Amended) A method according to claim 1, in which said step of forming at least one vertical spacer comprises forming a first vertical spacer in proximity to said front gate and having a bottom surface above said transistor body;
thereafter performing said step of etching said ~~Device~~ device layer to form said transistor body; and forming a second spacer in proximity to a vertical edge of said transistor body.

Claim 3 (Original) A method according to claim 1, in which said step of oxidizing said back gate electrode is performed with at least one vertical spacer disposed in proximity to a vertical edge of said transistor body, thereby defining a lateral extent of oxidation by the thickness of said vertical spacer, said oxidation extending underneath said vertical spacer and said transistor body and into said back gate electrode.

Claim 4 (Original) A method according to claim 2, in which said step of oxidizing said back gate electrode is performed with said second vertical spacer disposed in proximity to a vertical edge of said transistor body, thereby defining a lateral extent of oxidation by the thickness of said second vertical spacer, said oxidation extending underneath said vertical spacer and said transistor body and into said back gate electrode.

Claim 5 (Original) A method according to claim 1, further comprising a step of depositing a layer of interlevel dielectric about said transistor up to at least the top of said front gate, stripping said second vertical spacer, thereby forming an aperture over the source and drain of said transistor, and depositing a conductive material in said aperture, thereby forming a raised S/D structure.

Claim 6 (Original) A method according to claim 1, in which said step of oxidizing is conducted at a temperature of at least 1000 degrees Centigrade for a time sufficient to reduce stress in said transistor body.

Claim 7 (Original) A method according to claim 1, in which said step of oxidizing is conducted at a temperature of at least 1000 degrees Centigrade for at least twenty minutes.

Claim 8 (Original) A method according to claim 2, in which said step of oxidizing is conducted at a temperature of at least 1000 degrees Centigrade for at least twenty minutes.

Claim 9 (Original) A method according to claim 1, further comprising a step of performing an angled implantation into said back gate electrode of an ion species that promotes oxidation before said step of oxidation, thereby increasing the rate of oxidation in the implanted area.

Claim 10 (Original) A method according to claim 2, further comprising a step of performing an angled implantation into said back gate electrode of an ion species that promotes oxidation before said step of oxidation, thereby increasing the rate of oxidation in the implanted area.

Claim 11 (Original) A method according to claim 4, further comprising a step of performing an angled implantation into said back gate electrode of an ion species that promotes

oxidation before said step of oxidation, thereby increasing the rate of oxidation in the implanted area.

Claim 12 (Original) A method according to claim 6, further comprising a step of performing an angled implantation into said back gate electrode of an ion species that promotes oxidation before said step of oxidation, thereby increasing the rate of oxidation in the implanted area.

Claim 13 (Original) A method according to claim 7, further comprising a step of performing an angled implantation into said back gate electrode of an ion species that promotes oxidation before said step of oxidation, thereby increasing the rate of oxidation in the implanted area.

Claim 14 (Original) A method according to claim 1, further comprising a step of performing a vertical implantation into said back gate electrode of an ion species that retards oxidation before said step of oxidation, thereby decreasing the rate of oxidation in the vertical direction.

Claim 15 (Original) A method according to claim 6, further comprising a step of performing a vertical implantation into said back gate electrode of an ion species that retards oxidation before said step of oxidation, thereby decreasing the rate of oxidation in the vertical direction.

Claim 16 (Original) A method according to claim 7, further comprising a step of performing a vertical implantation into said back gate electrode of an ion species that retards oxidation before said step of oxidation, thereby decreasing the rate of oxidation in the vertical direction.

Claim 17 (Original) A method according to claim 13, further comprising a step of performing a vertical implantation into said back gate electrode of an ion species that retards oxidation before said step of oxidation, thereby decreasing the rate of oxidation in the vertical direction.

Claim 18 (Original) A method of forming a double-gate transistor comprising the steps of:

providing an SOI wafer having a first substrate, a BOX layer and a device layer;

forming a back gate dielectric layer on said device layer;

forming a back gate electrode on said back gate dielectric layer;

bonding a second wafer having a second substrate to said back gate electrode of said SOI wafer;

removing said first substrate;

removing said BOX layer;

forming a front gate dielectric on said device layer;

forming a front gate electrode layer on said front gate dielectric layer;

depositing at least one transfer layer on said front gate dielectric;

patterning said at least one transfer layer with a gate pattern and forming a first gate in said front gate electrode layer;

forming at least one vertical spacer layer adjacent to opposite sides of said first gate;

etching said device layer using said at least one spacer layer as a mask to form a transistor body disposed on said back gate dielectric layer;

oxidizing said back gate electrode such that oxide is formed below said transistor body and on either side of a central portion of said back gate electrode, thereby forming said back gate self-aligned with said first gate; and

forming source and drain electrodes on opposite sides of said transistor body.

Claim 19 (Withdrawn) A double-gate transistor formed in a semiconductor wafer having a substrate and a device layer, said transistor comprising:

a back gate dielectric layer below said device layer;

a back gate electrode below said back gate dielectric layer;

a front gate dielectric above said device layer;

a front gate electrode layer above said front gate dielectric layer and vertically aligned with said back gate electrode;

a transistor body disposed above said back gate dielectric layer, symmetric with said first gate, said back gate electrode having a layer of oxide formed below said transistor body and on either side of a central portion of said back gate electrode, thereby positioning said back gate self-aligned with said front gate; and

source and drain electrodes on opposite sides of said transistor body.

Claim 20 (Withdrawn) A transistor according to claim 19, in which conductive S/D contact members are disposed above said source and drain electrodes, extending above said front gate dielectric to a contact surface at a height less than said front gate electrode.